SiC FAQ

Silicon Carbide Frequently Asked Questions

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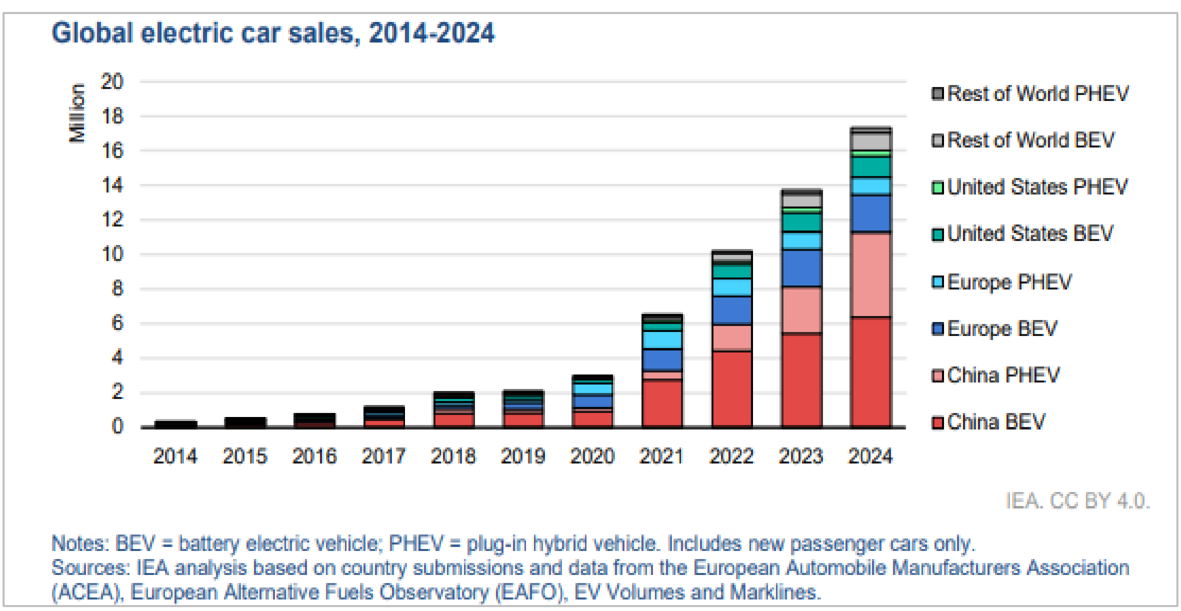
DB HiTek

Q1) SiC says that the main market is electric vehicles and the recent electric vehicle market is not good, so isn't it oversupply to advanced competitors who have already entered?

A1) SiC, a high-power device with superior characteristics compared to Si, has low power loss and is very good for high-temperature/high-speed operation. (3x the thermal conductivity, 10x the insulation breakdown electric field strength) This simplifies the size/weight of the final system as well as the chip size of the product makes it feasible (reducing fuel efficiency/low carbon emissions from eco-friendly cars)

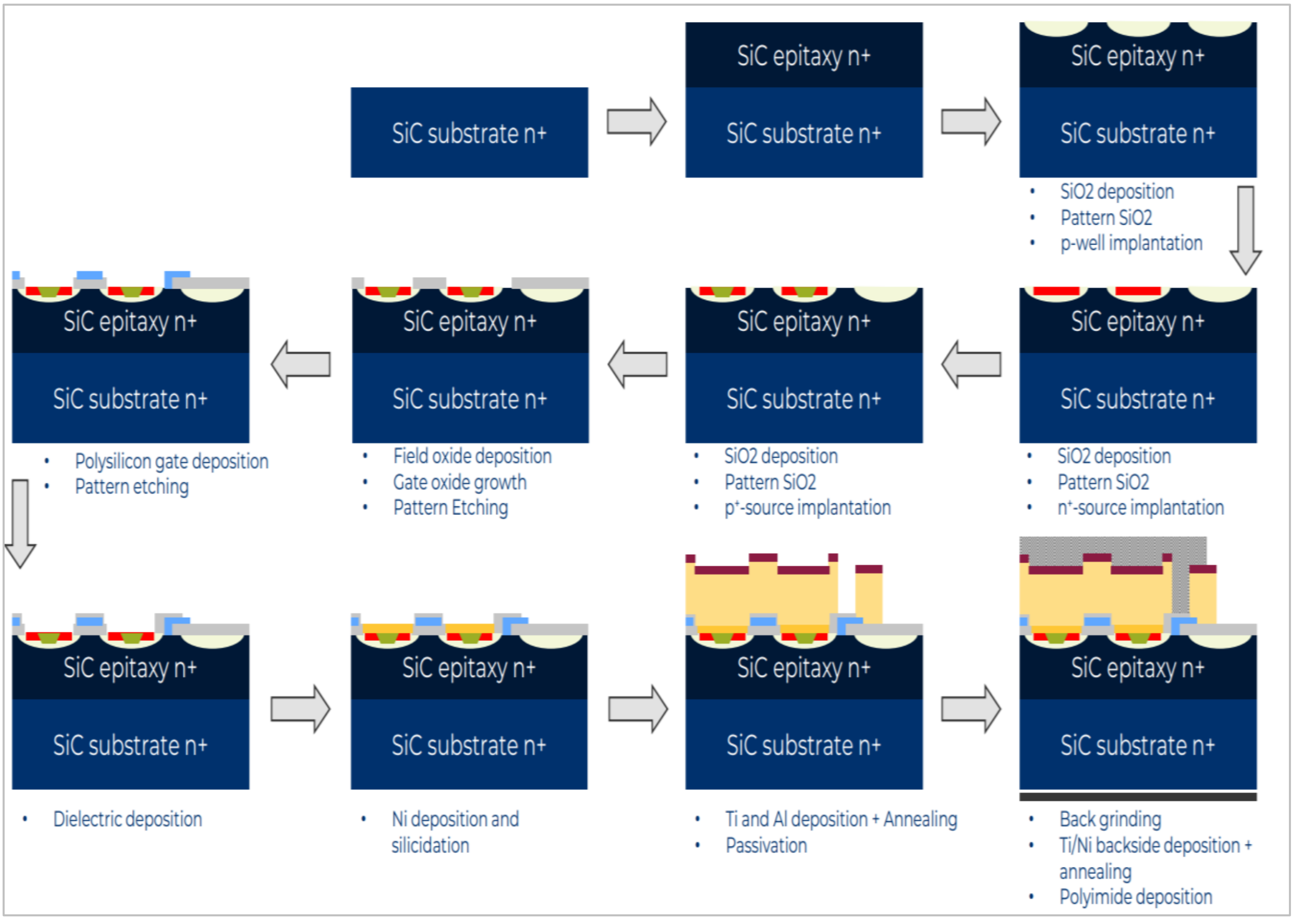
Source: SK siltron, Maeil Business Newspaper

In the case of the electric vehicle market, it grew rapidly (50%) by '23 compared to FCST, but in the case of '24 years, lack of charging infrastructure, high prices, high interest rates, Although the abolition of subsidies is showing signs of modest growth (16%), each country's low carbonization policies (carbon neutral 2050) The FCST of long-term growth remains unchanged on the back. (EU : Green Deal, CHN : Zero Carbon, US : Clean Energy)



Q2) What is the difference between Si and SiC from the process point of view?

A2) In the case of silicon, it can be manufactured by introducing a manufacturing device from the outside and baking a circuit thinly on the silicon surface that becomes the substrate, but in the case of SiC/GaN power devices, the composition must be changed by ion implantation and then deposited in several layers before the substrate must be dug deep from top to bottom. It is a technology that requires knowledge-how accumulated over a long period of time, such as at what temperature and for how long to process. It is a technology system that requires analog product technology, not the same performance, even if you make the same thing with the same device, the same material, and the same shape.
In particular, regarding the ion implantation technology, the Si ion implanter is evaluated to be high-temperature, but the SiC process uses Al, which is difficult to handle as an ion species, and a high temperature implantation of several 100° C is required to prevent amorphousization in the High Dose implantation. It is very different from Si that high temperature annealing at 1,600° C or higher is indispensable to resolve residual defects, so a SiC-only process is required as follows.



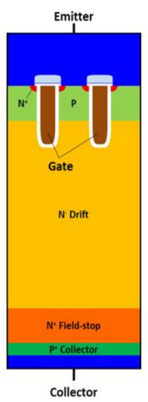
Source: Yole Power SiC 2023

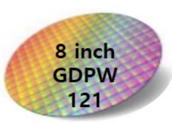
Q3) SiC is many times more expensive, but small-sized chips. Why do you use them in parallel?
(IGBT only needs to use one 1200V 200A x 1 chip, but does SiC MOSFET use 1200V 50A x 4 chips parallels, 4 times as much?)

A3) As you can see in answer 1, SiC can reduce the system size and weight of electric vehicle system due to its excellent characteristics. If the chip size is the same, SiC can be used to make higher current at high temperature. On the other hand, the higher the chip size due to the higher defect density of SiC raw material, the lower the product yield, which makes it difficult to secure mass productivity with current technology.

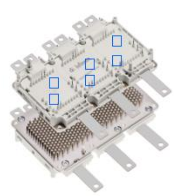
Si vs SiC Products (Below : Chip size, GDPW, Yield)

Si IGBT



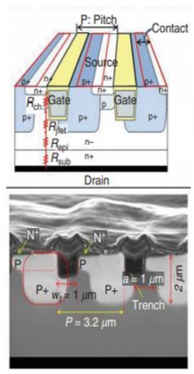


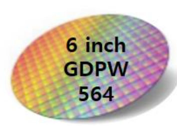
Chip size
16mm x 12mm
192mm²
Yield 80%



1200V, 200A
x 6 chips/ Module

SiC MOSFET





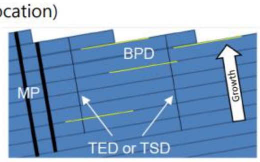
Chip size
5mm x 5mm
25mm²
Yield 50~60%

1200V, 200A
(50A x 4병렬)
x 24 chips /Module

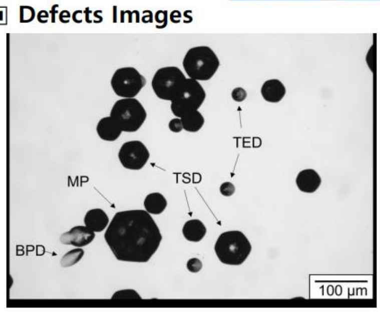
- Reference : Analyzed Data sheet Real chip size measurement by DBH Marketing
  IEEE Magazine, 2329-9207/19, White paper by Peter Fridrichs (IFX VP of SiC)

▣ Crystal Defects(Bare Wafer)

1) TSD(Threding Screw Dislocation)
2) MP(Micro Pipe)
3) TED(Threding Edge Dislocation)
4) BPD(Basal Plane Dislocation)

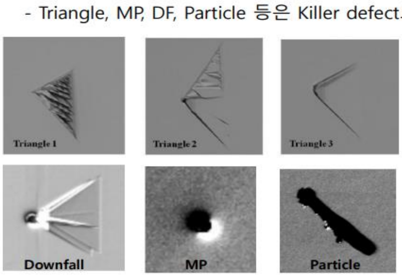


▣ Defects Images

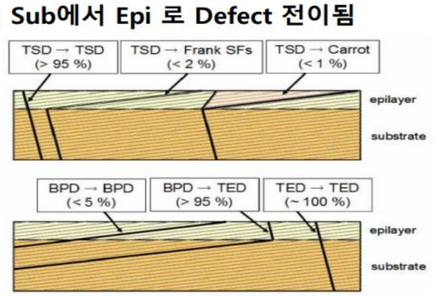


▣ Epi Defects

- Triangle, MP, DF, Particle 등은 Killer defect으로 알려져있음.



▣ Sub에서 Epi 로 Defect 전이됨



Q4) How to improve the current density of SiC?

I understand that we can use high pressure characteristics and current density due to wide band gap and high heat conduction, but I wonder how to make it possible to use higher current density. Is there a way to increase the current density by raising Vgs more than Si or is there another way? (I know it is not higher than Si in terms of channel mobility, and higher in terms of saturation velocity, but I wonder how to increase the current density.

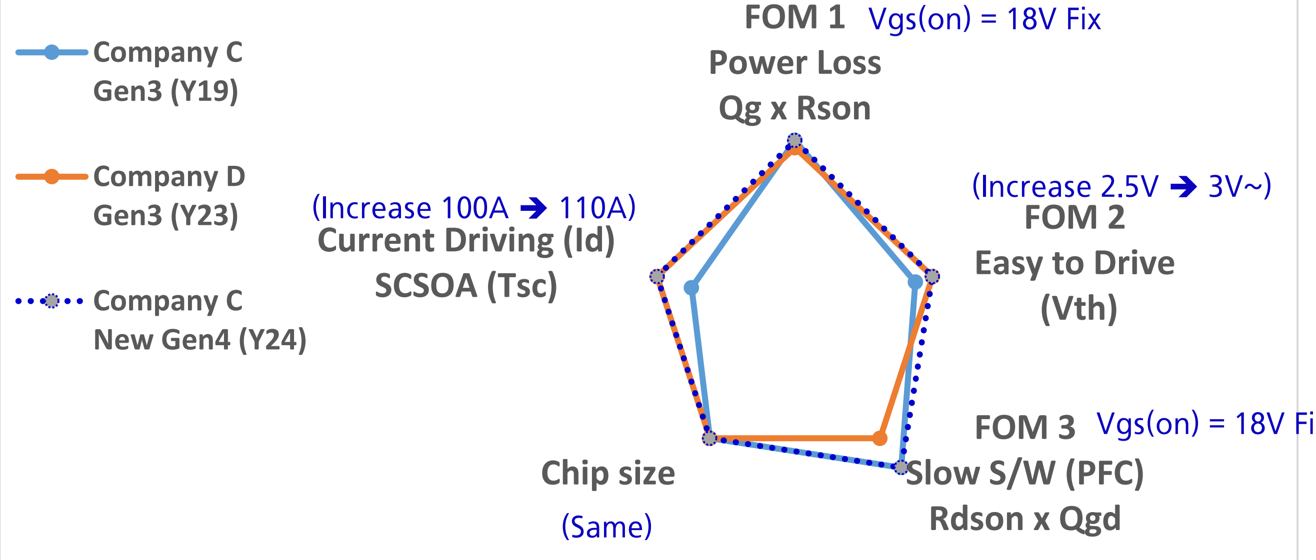
A4) Make the most of your strengths at high temperatures and maximize Channel density structurally

I agree with you that Si has better channel mobility than SiC and is more advantageous for increasing current density. However, among the many reasons why people who do SiC have good current density of SiC.... As a reasonable story, there are the following contents.

- This is because SiC characteristics make it easier to reduce the chip size as it goes to high voltage, and SiC's current driving loss is small at high temperatures.
- For example, if 1200V 100A current spec is measured at 100C at the same room temperature at 25C, Si IGBT is halved by 50% to 50A, and SiC is halved by 70% to 75A.

A general way to improve the current density of SiC MOSFET 1.2kV products is

- While maintaining the same chip size as before, Rsp is reduced to improve the Rdson while increasing the current density at high temperatures. In traditional Si, the difference is that the Rdson is reduced and the Chip size is reduced.
- The disadvantage of SiC is that if the chip size is reduced, the thermal resistance Rthjc is poor and the smaller chip generates more heat, so there is a limit to reducing it beyond the appropriate limit. As a result, technology that can improve the cooling system of the power module package is also being developed.



Q5) Why and how do you do Burn In Screen Test at Wafer Level, which doesn't exist in Si?

A5) Compared to silicon, silicon carbide has an external defect density three to four times higher in gate oxide due to a higher electrical defect density, so SiC re-examinations commercialize a device that matches Vth and RDS(on) after a Burn In Screen Test.
If only the probing test is performed at the Wafer Level, as shown in the figure below, and the Chip YLD is 90%
This is because the module product (36 chips) CUM Yield falls to the 3% level, making it difficult to commercialize it

Burn In Screen을 하지 않았을 때, Yield 동향

Die Yield**	Module Yield with 12 Dies	Module Yield with 36 Dies
99%	89%	72%
98%	78%	52%
90%	28%	3%

Burn-In test is a process that detects the initial failure of a component, so it increases the reliability of the component. Burn-In test is a reliable and actionable way to increase product reliability
During the Burn-In test, the components operate under extreme operating conditions (i.e. elevated temperature and voltage)

Wafer size	6", 8" wafer
Burn-in type	HTGB, HTRB
Dimension	2800(W) X 2400(H) X 4500(D)
Power	<30kW(Max)
Temperature	RT - 175℃
Voltage	Gate ±75V, Drain 2000V
Voltage accuracy	±75V 0.1%+0.2V 2000V 0.5%+10V
Current range	Gate 100nA/1uA/10uA/100uA Source1uA/10uA/100uA/1mA
Current accuracy	100nA 1%+0.5nA 1uA 0.1%+1nA 10uA 0.1%+5nA 100uA 0.1%+10nA 1mA 0.1%+50nA

Q6) I heard HV H3TRB and SiC Module have a standard called AQG-324 in the reliability test of SiC products, so please explain

A6) The Qual of high-power devices is divided into AEC-Q101 (Discrete Device) and AQG-324 (Module). Both standards are vehicle reliability assessments, conditions, quantities, and criteria, with some similar items, but AQG-324 has higher evaluation item coverage.
As mentioned in Q5's Burn-in Test, it is more difficult to evaluate and verify reliability after module production because the defect rate is higher when it is a module than when it is a Discrete.
The table below shows the reliability assessment items and conditions expressed in AEC-Q101 and AQG-324.
Green shows a similar (or identical) evaluation, while red shows a different evaluation.
HTRB, HTGB, and H3TRB are the most important reliability assessments, and DRB (Dynamic HTRB), DGB (Dynamic HTGB), and Dynamic H3TRB are the evaluations that have been developed to fit more practical use environments.
Dynamic evaluation is usually performed by actively turning on/off the element along with the gate drive and can be evaluated as a module. (DRB and DGB can also be evaluated as Discrete)

- **AEC-Q101 (Auto Electronics Council)**

항목	조건
TC	-55~150
HAST	130/85%/max. 42V)/96hrs
UHAST	130/85%/96hrs
AC	121/100%
ACBV	AC Blocking Voltage
HTRB	max Tj/max V (Adjust Ta to avoid thermal runaway)
HTGB	max Tj/max gate bias (posi, nega)
H3TRB	85/85%/max. 100V/1000hrs
IOL	dT≥100
PTC	IOL (small)

- **AQG-324 (European Center for Power Electronics)**

항목		조건
TST	Thermal Shock Test	-40~125
CO	Contactability	-
V	Vibration	-
MS	Mechanical Shock	-
HTRB	High Temp Reverse Bias	max Tj / ≥80% VD
DRB	Dynamic Reverse Bias	RT / ≥80% VD / f ≥ 25kHz (off state)
HTGB	High Temp Gate Bias	VGS,min/max / 50% DUT Positive, Negative
DGS	Dynamic Gate Stress	RT / Vg : min/max / f>50kHz (D>20%)
H3TRB	High Humidity, Temp Reverse Bias	
dyn. H3TRB	Dynamic H3TRB	Vds>0.5Vds,max / >30V/nsec / 15~25kHz
HTFB	High Temp Forward Bias	Body Diode Test
dyn. HTFB	Dynamic HTFB	-
PC(sec)	Power Cycle (<5sec)	≤5sec, 85% ID, Coolant flow
PC(min)	Power Cycle (>15sec)	≥15sec, 85% ID, Coolant flow
HTS	High Temp Storage	≥125'C
LTS	Low Temp Storage	≤-40

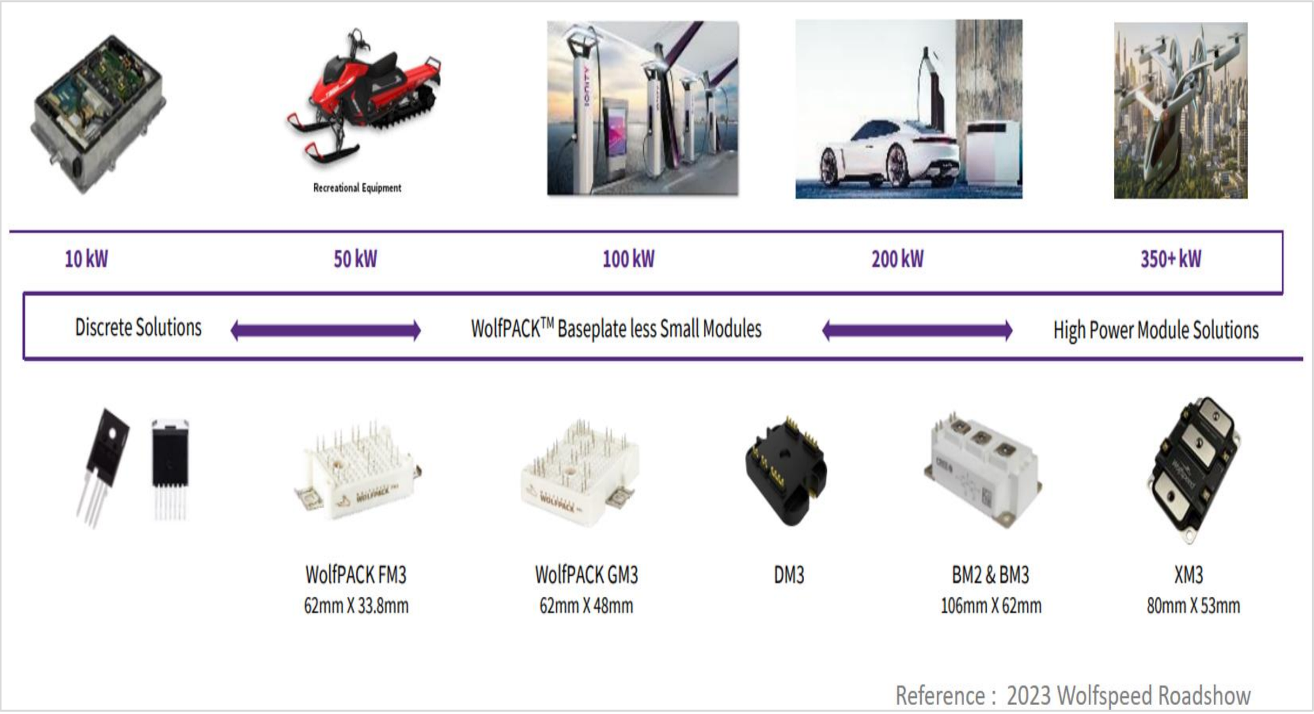
HV-H3TRB is not an evaluation condition specified in the standard, but it is a condition required/presented by Automotive, led by Infineon. WBG devices such as SiC and GaN are demanding a new standard (Beyond AEC-Q101) that goes beyond the existing Si-based standard, and as part of that, the evaluation time increase (1008hrs ➔ 2000hrs) of the existing evaluation (HTRB, HTGB, H3TRB) or HV-H3TRB (HTRB+H3TRB).

Table 3 Selected test conditions for automotive qualificat

Qualification test conditions (examples)	
AEC-Q101	Automotive SiC (beyond AEC-Q101)
H3TRB @ 80–100 V	HV-H3TRB @ › 80% V_{DSS}
Static H3TRB @ 80–100 V	Dynamic (HV)H3TRB › f = typical switching frequency › $V_{DS,app}$

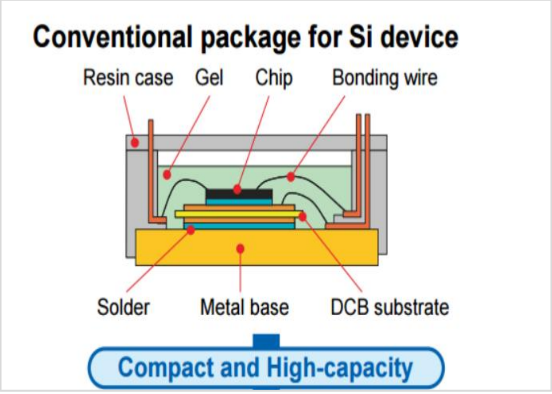
Q7) I would like to know about SiC products, major applications, and product development trends of advanced companies aimed at DB HiTek?

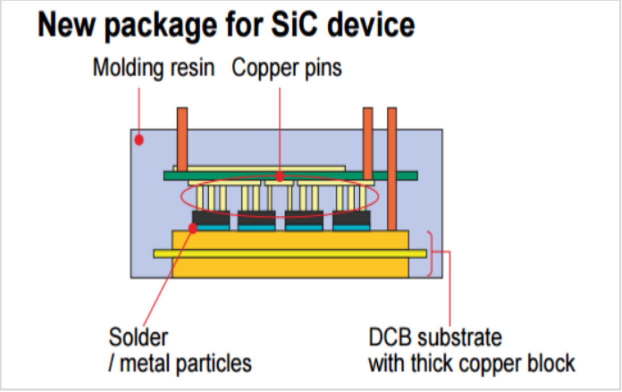
A7) The product line-up is equipped according to the system output power of each application, and SiC is being developed mainly for high output modules of 200kW or more.
Discrete is applied as a design flexibility and cost-saving strength in systems under 50kW (OBC, Light-Vehicle) High-power systems are developed optimized for Small Module > High Power Module characteristics depending on the SiC Power Density of the module product



Source: Wolfspeed 2023 Roadshow

As a new product development trend, a half bridge module of double-sided cooling power module with excellent cost-effectiveness and product characteristics is being developed





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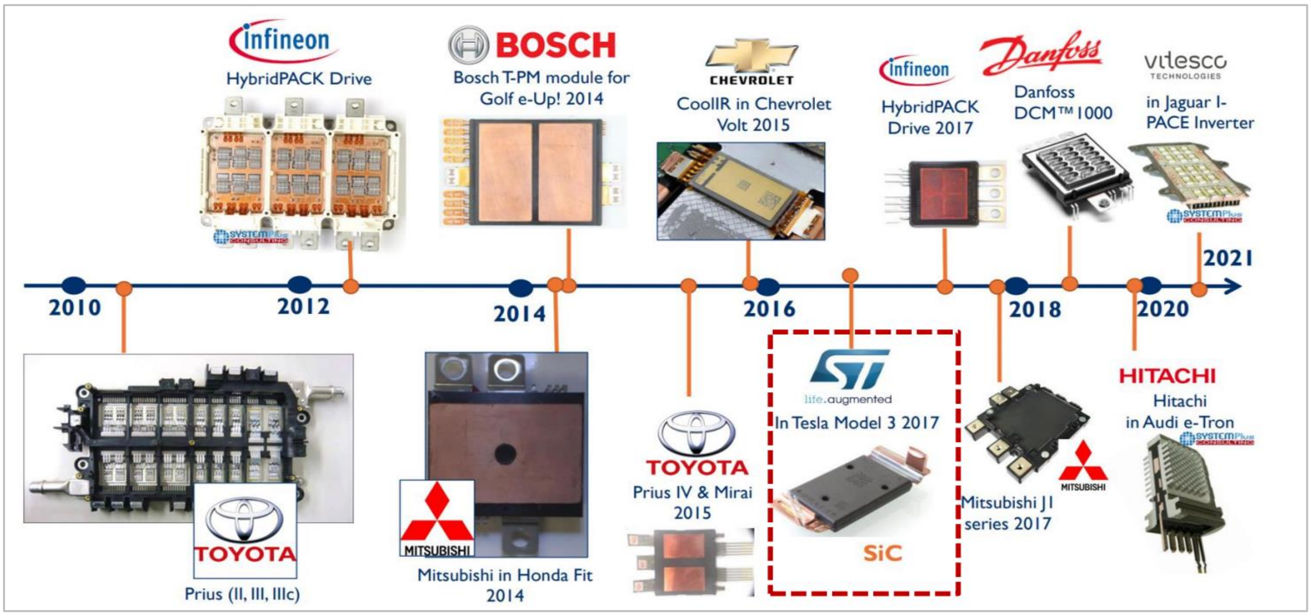
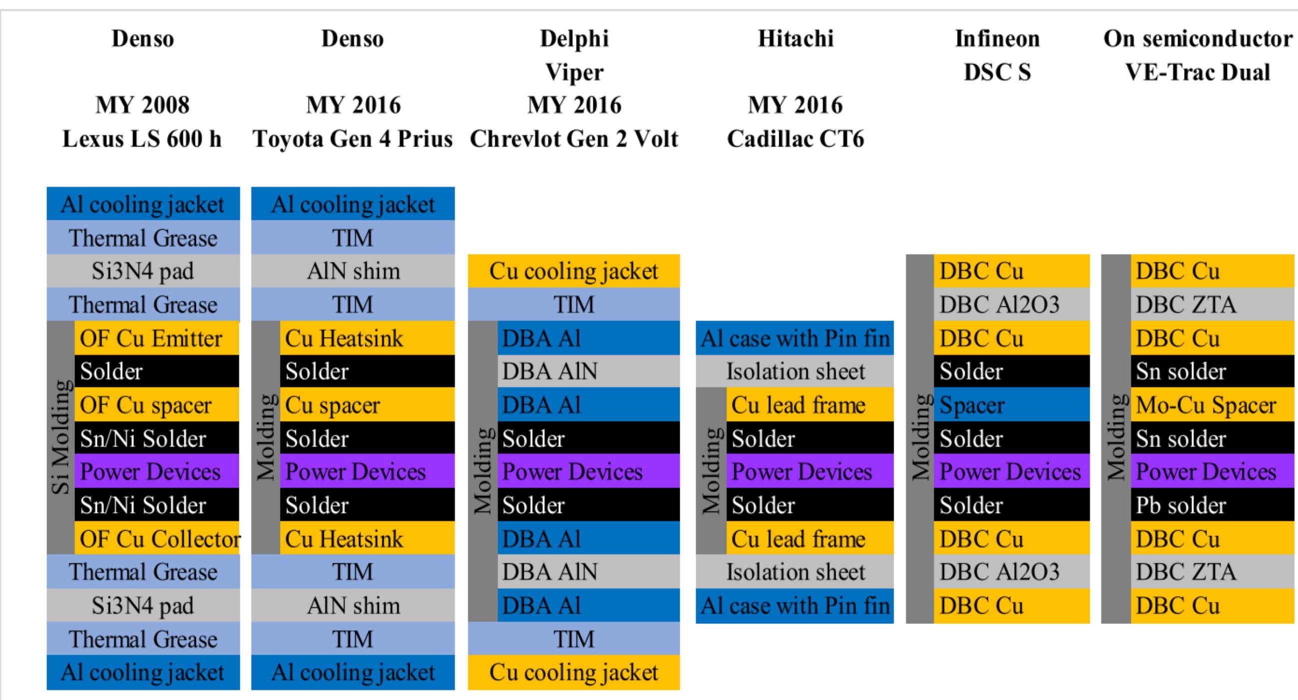
As shown in the figure below, a customized module product is being developed by the vehicle manufacturer/module product company (IDM/Fabless), which requires the design to create a compact SiC-only module optimized for SiC devices

HiTec is preparing a customized metal process (Solderable metal) for support according to different module products for each customer,

In addition, as mentioned in Q6, for SiC module chip business, we aim to develop products that meet the module product Qualified AQG-324.





Source : IEEE, Automotive Power Module Packaging : Current Status and Future Trends